Verifiable ASICs: trustworthy hardware with untrusted components

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Untrusted manufacturers can craft hardware Trojans

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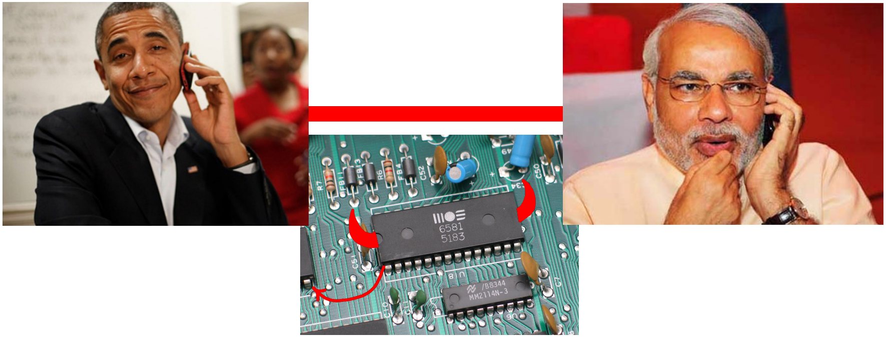

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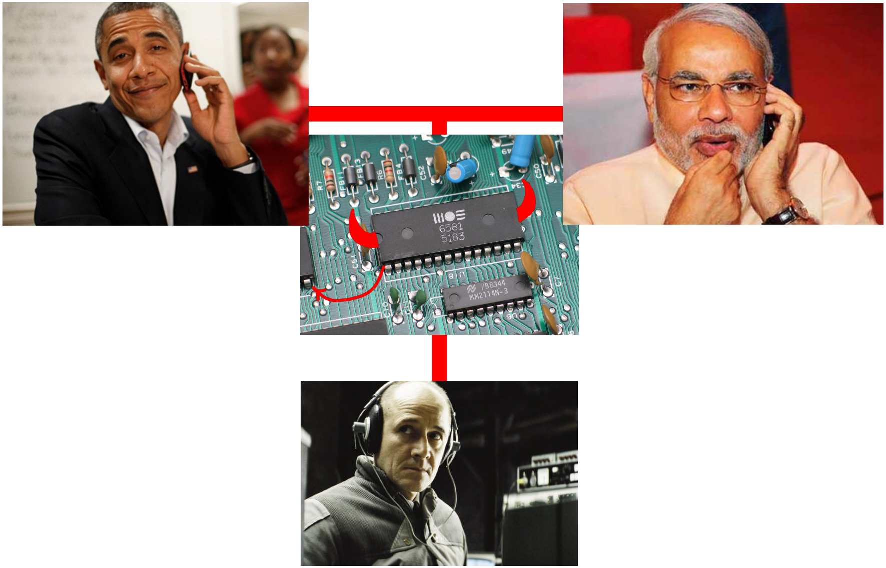

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Trusted fabrication is not a panacea:

- ✗ Only 5 countries have cutting-edge fabs on-shore
- ✗ Building a new fab takes \$\$\$\$\$\$, years of R&D
- ✗ An old fab could mean $10^8\times$ performance hit accounting for speed, chip area, and energy

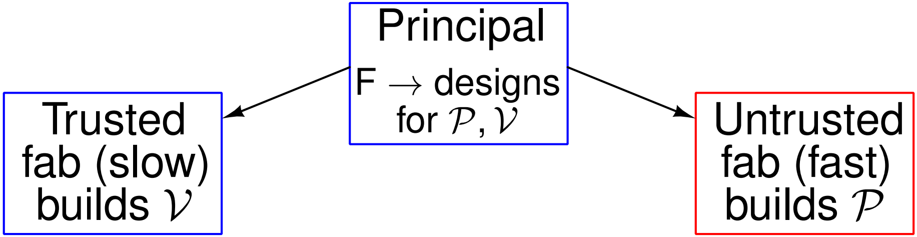
Can we get trust more cheaply?

Can we build Verifiable ASICs?

Principal

F $\rightarrow$ designs for $\mathcal{P}, \mathcal{V}$

Can we build Verifiable ASICs?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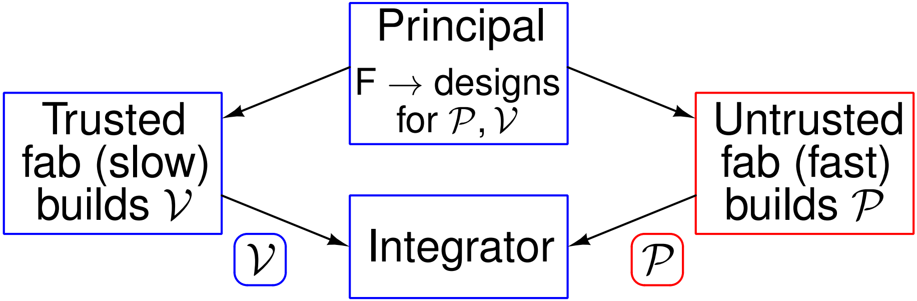

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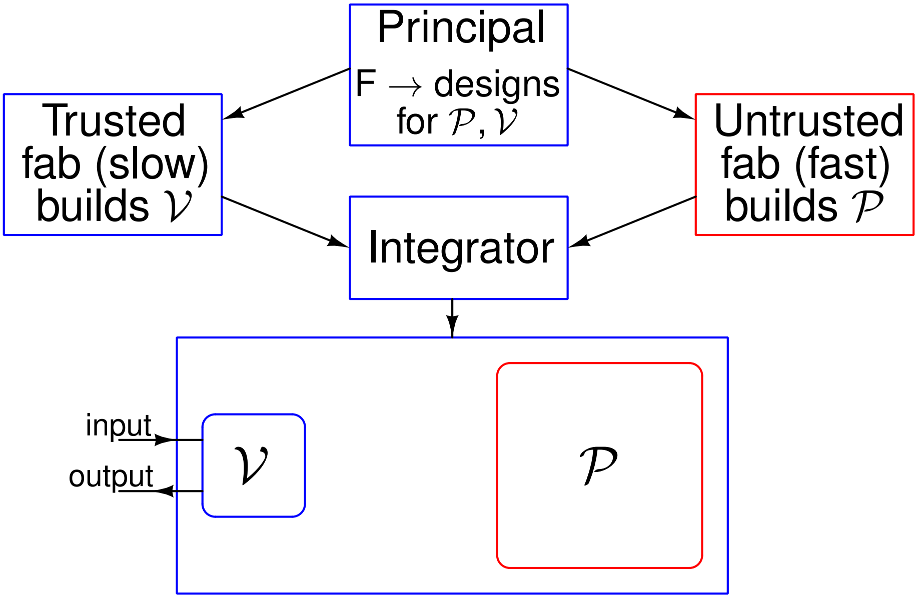

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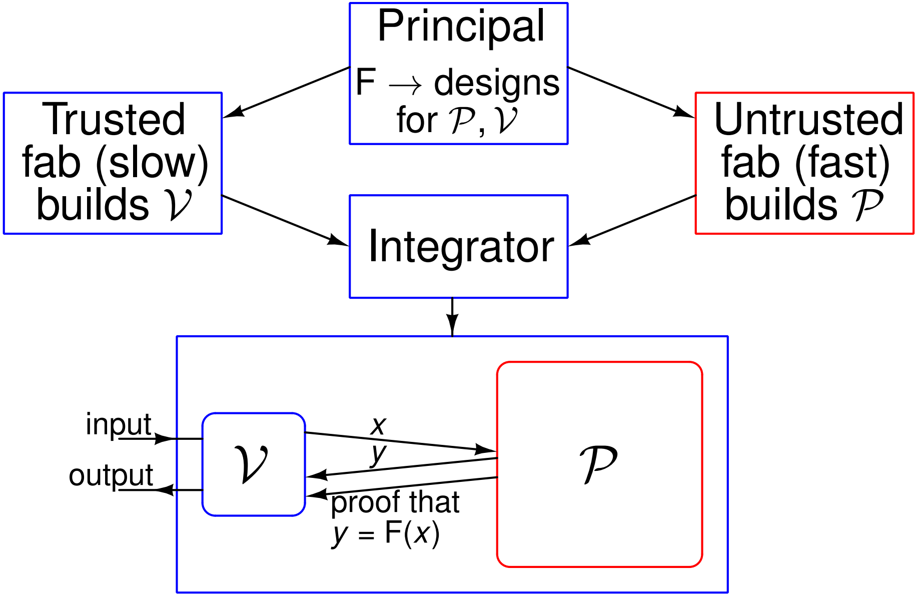

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F $\rightarrow$ designs for $\mathcal{P}$, $\mathcal{V}$
Trusted fab (slow) builds $\mathcal{V}$
Untrusted fab (fast) builds $\mathcal{P}$
Integrator
input
output
$\mathcal{V}$
x
y
proof that $y = F(x)$
$\mathcal{P}$

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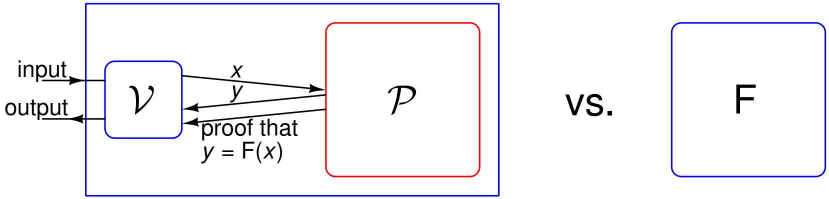

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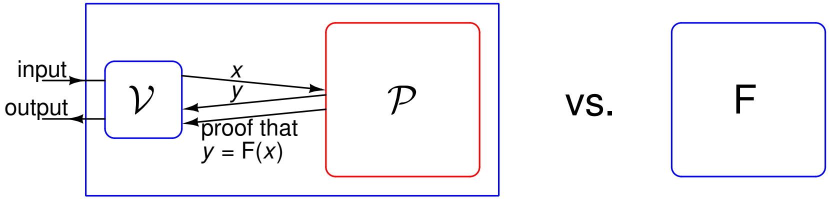

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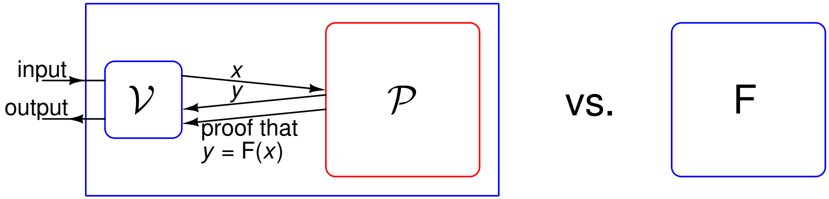

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- Reasons for hope:
  - running time of $\mathcal{V} <$ running time of F (asymptotically)
  - speed of cutting-edge fab might offset $\mathcal{P}$'s overheads
- Challenges remain:
  - Hardware issues: energy, chip area
  - Need physically realizable circuit design
  - $\mathcal{V}$ needs to save work at plausible computation sizes

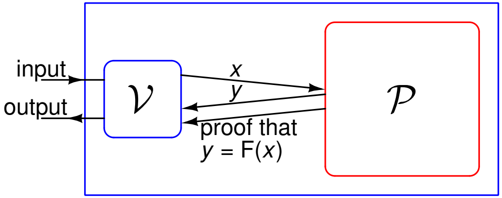
Zebra: a hardware design that saves costs

A **qualified** success

Zebra: a hardware design that saves costs. . .

. . . sometimes.

Probabilistic proof systems, briefly



F must be expressed as an arithmetic circuit (AC)

generalized boolean circuit over $\mathbb{F}_p$

$\wedge \rightarrow \times \qquad \vee \rightarrow +$

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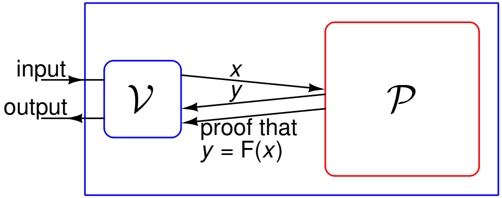

F must be expressed as an arithmetic circuit (AC)

AC satisfiable $\iff$ F was executed correctly

$\mathcal{P}$ convinces $\mathcal{V}$ that the AC is satisfiable

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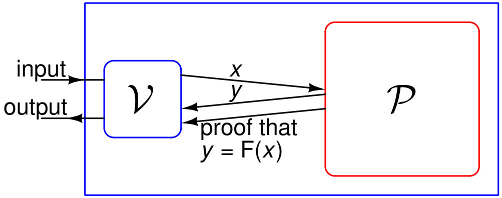

Arguments [GGPR13, SBVBPW13, PGHR13, BCTV14]

e.g., Zaatar, Pinocchio, libsnark

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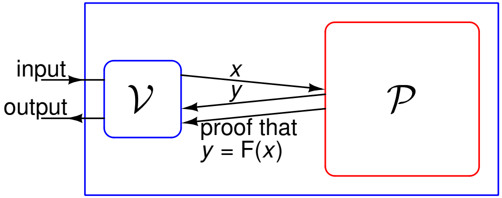

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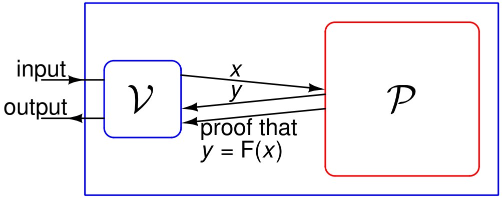

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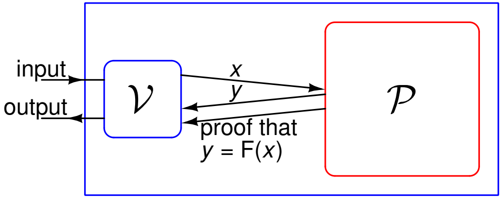

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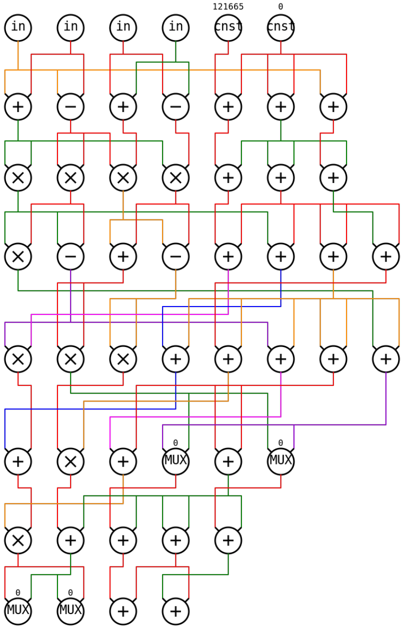
Suited to hardware implementation ✓

Zebra builds on IPs of GKR [GKR08, CMT12, VSBW13]

F must be expressed as a *layered* arithmetic circuit.

Note: this is an abstraction of F, *not* a physical circuit!



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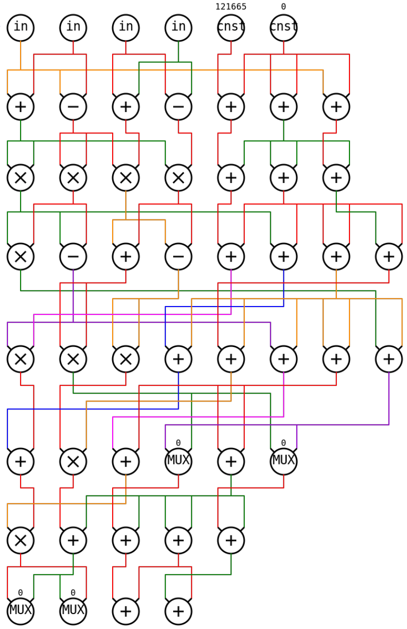

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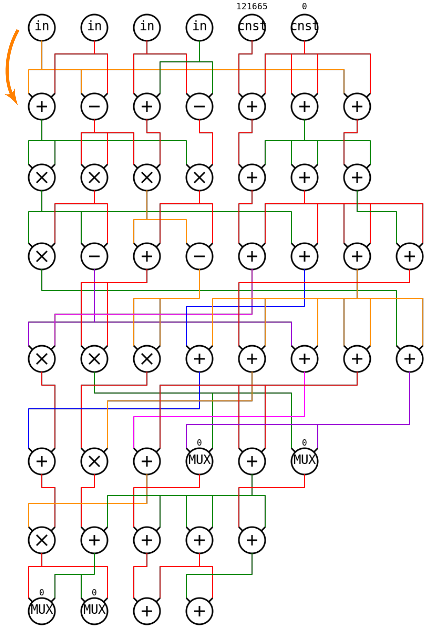

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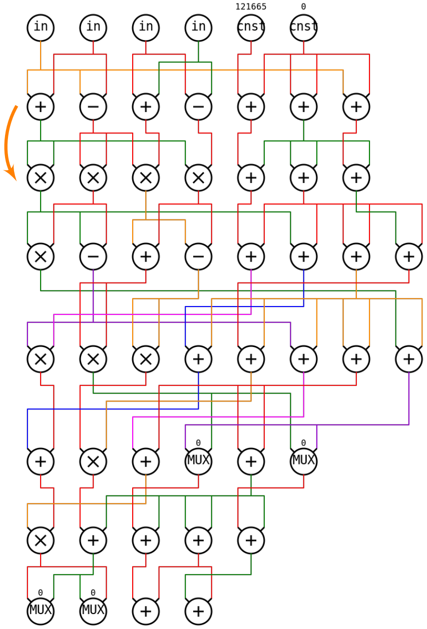

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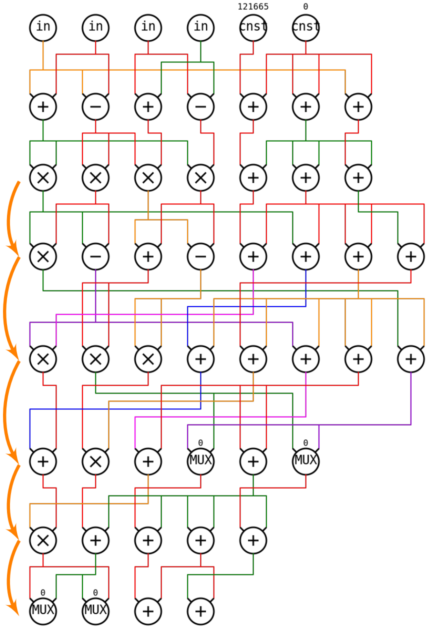

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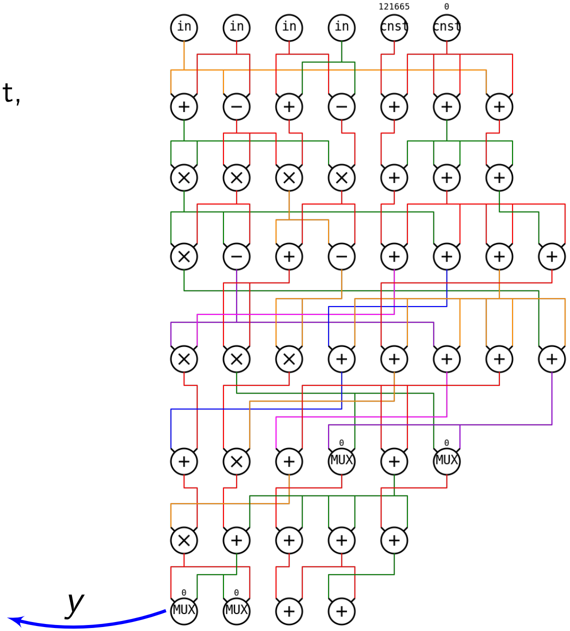

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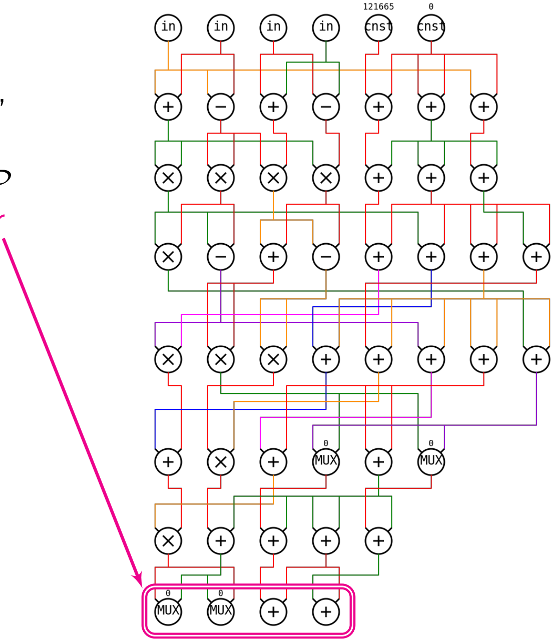

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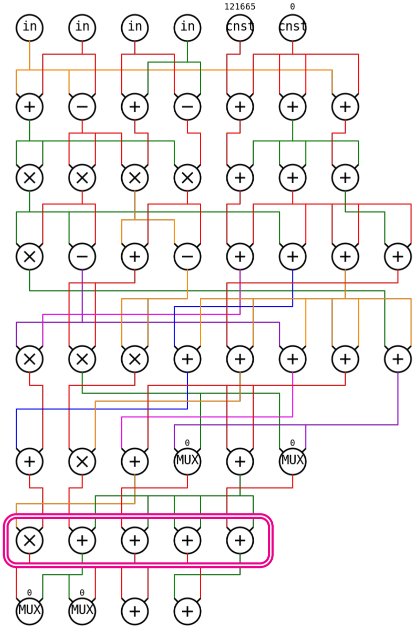

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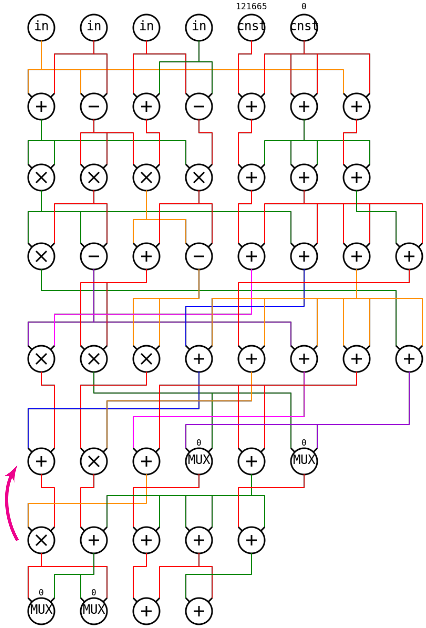

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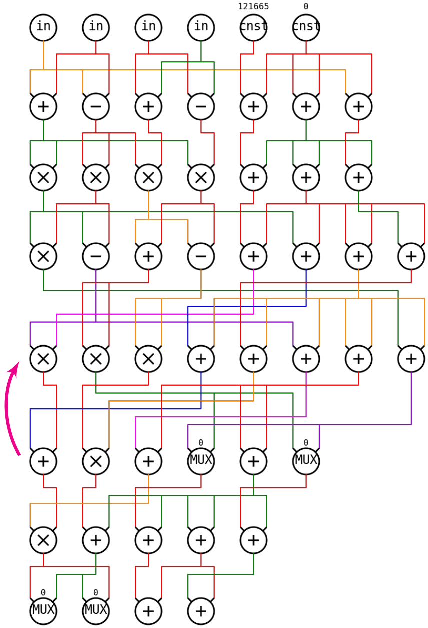

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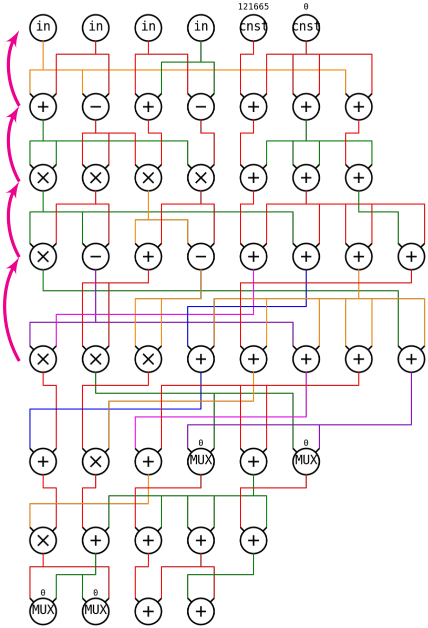

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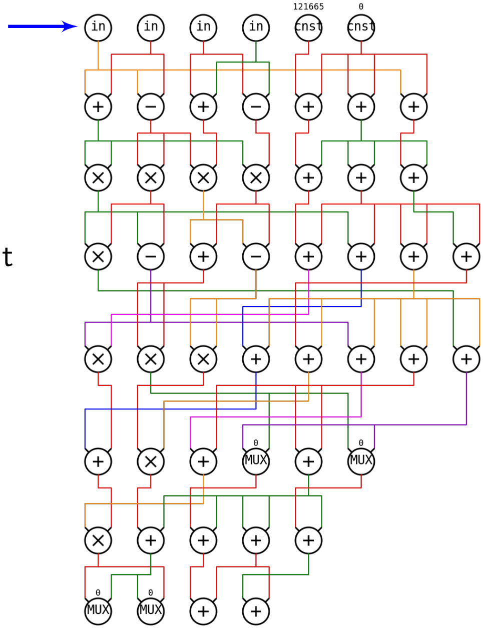

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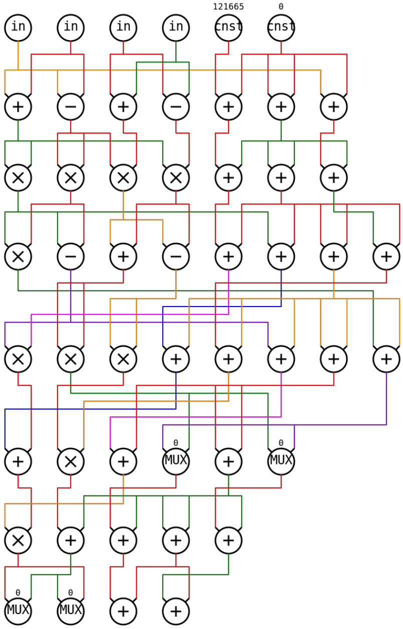
4. $\mathcal{V}$ iterates, ends up with claim about inputs
5. $\mathcal{V}$ checks consistency with the inputs

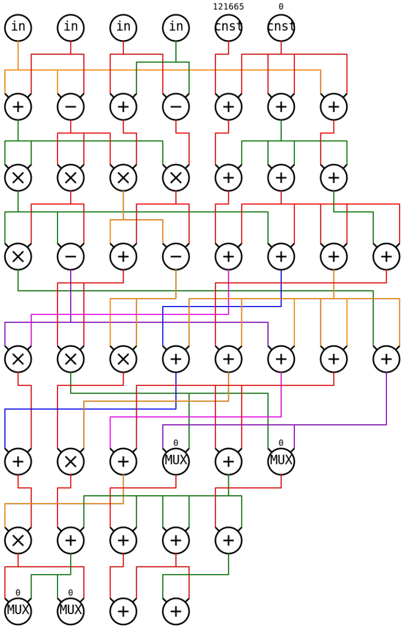
$\mathcal{V}$'s work $\approx O(\text{depth} \cdot \log \text{width})$, so it saves work when width $\gg$ depth



Can we parallelize this interaction?

Can $\mathcal{V}$ and $\mathcal{P}$ interact about all of F's layers at once?

No. $\mathcal{V}$ must ask questions in correct order or $\mathcal{P}$ can cheat!



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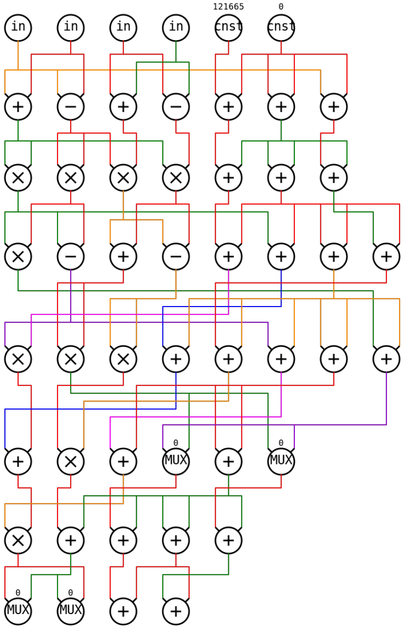
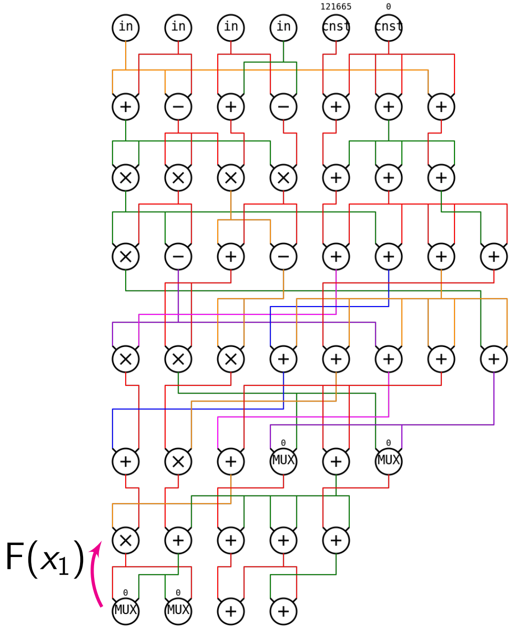
But: Zebra uses pipelining to parallelize several Fs.



Extracting parallelism through pipelining

$\mathcal{V}$ questions $\mathcal{P}$ about $\mathrm{F}(x_1)$'s output layer.



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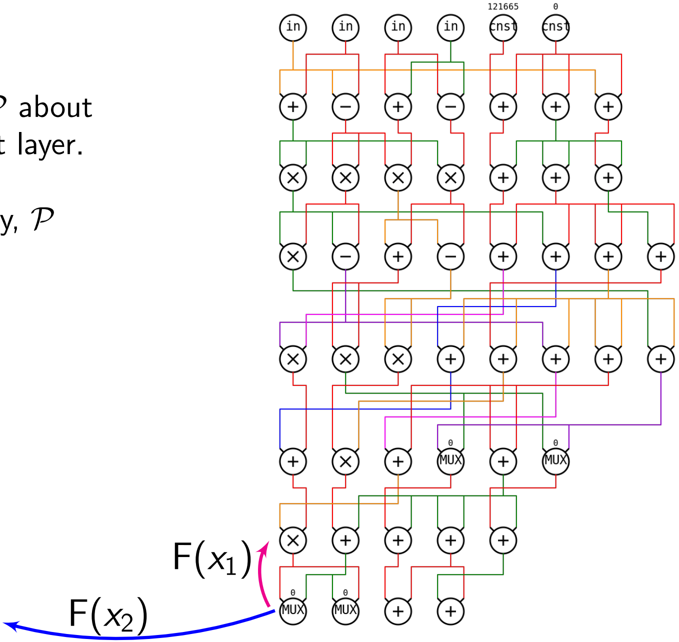
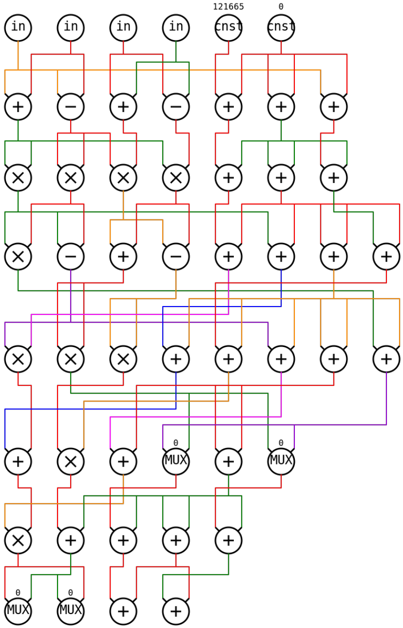
Simultaneously, $\mathcal{P}$ returns $\mathsf{F}(x_2)$.



Extracting parallelism through pipelining

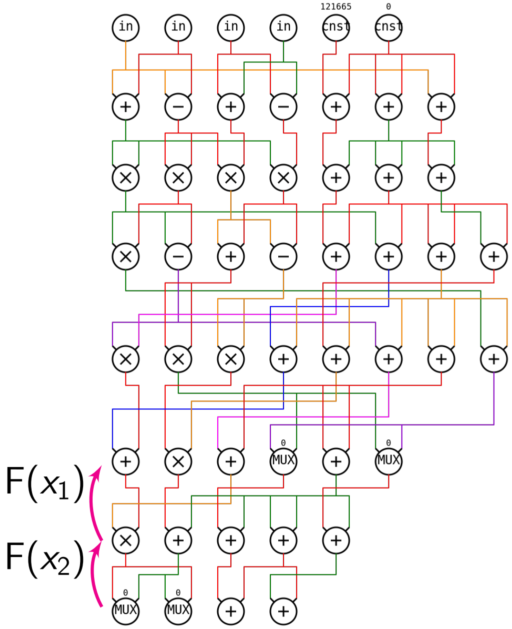
$\mathcal{V}$ questions $\mathcal{P}$ about $F(x_1)$'s next layer



$F(x_1)$

Extracting parallelism through pipelining

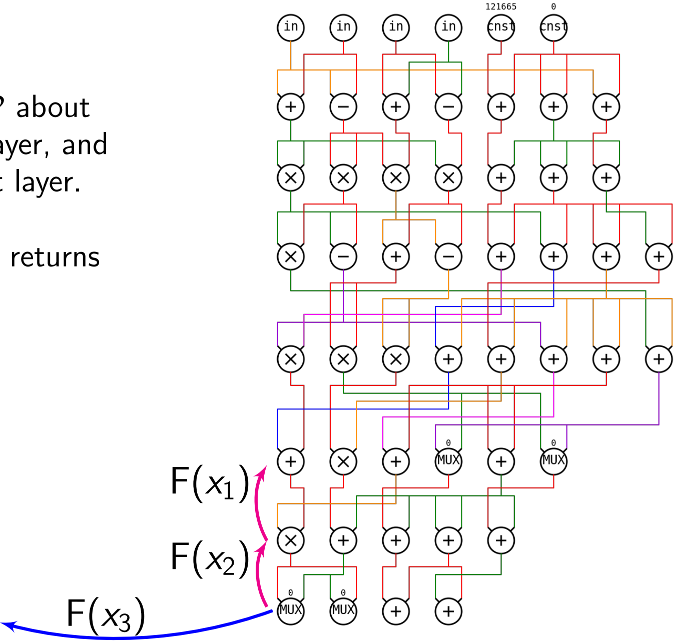
$\mathcal{V}$ questions $\mathcal{P}$ about F(x_1)'s next layer, and F(x_2)'s output layer.



Extracting parallelism through pipelining

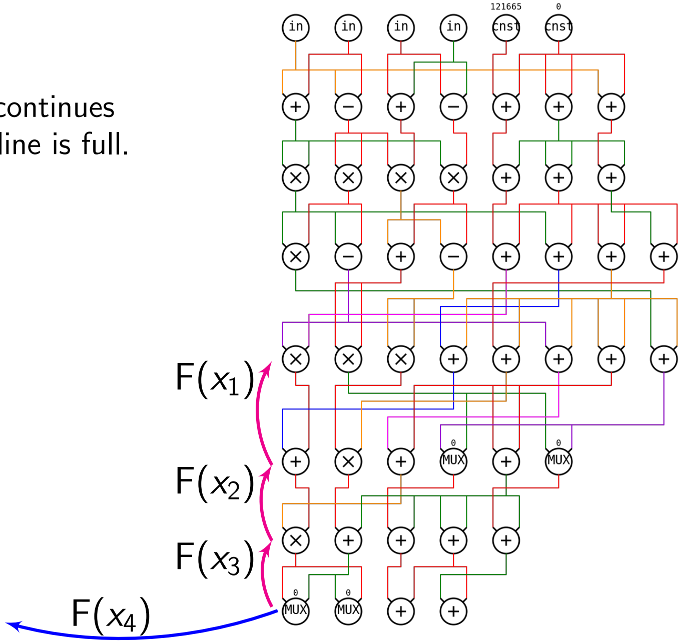
$\mathcal{V}$ questions $\mathcal{P}$ about $F(x_1)$'s next layer, and $F(x_2)$'s output layer.

Meanwhile, $\mathcal{P}$ returns $F(x_3)$.



Extracting parallelism through pipelining

This process continues until the pipeline is full.



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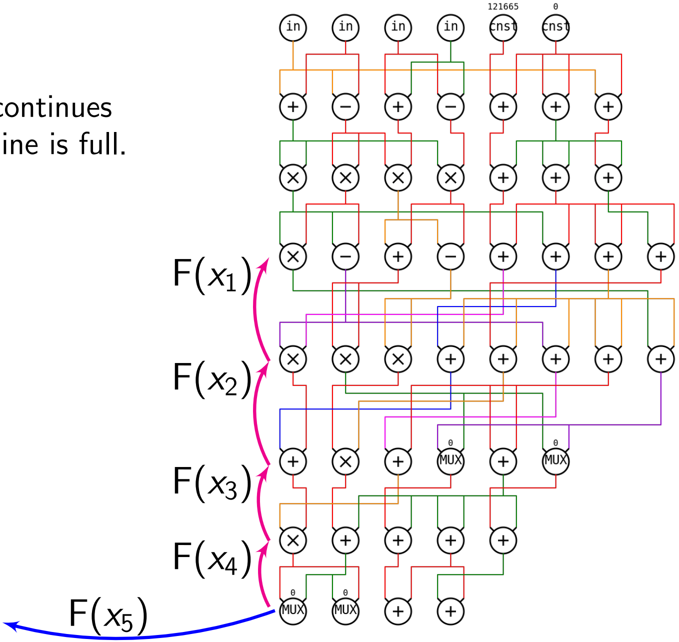
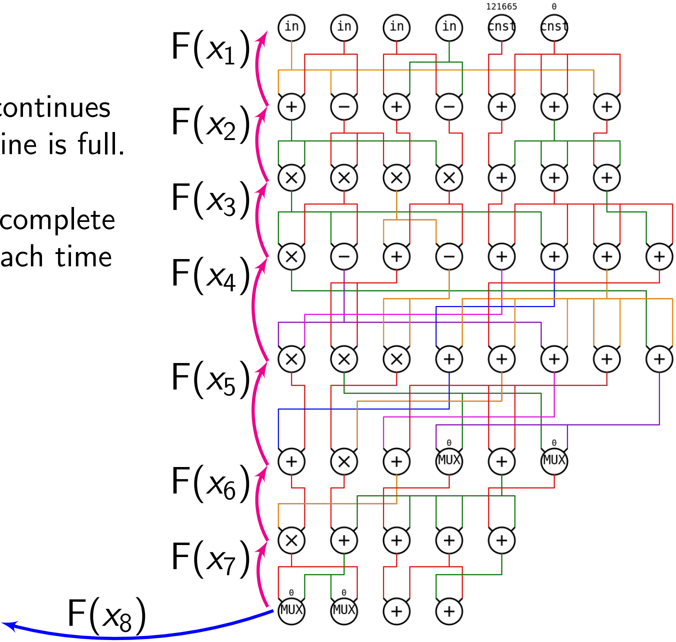


Extracting parallelism through pipelining

This process continues until the pipeline is full.

$\mathcal{V}$ and $\mathcal{P}$ can complete one proof in each time step.



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✓ Reduce, reuse, recycle

e.g., computation: save energy by adding memoization to $\mathcal{P}$
e.g., hardware: save chip area by reusing the same circuits

Architectural challenges

Interaction between $\mathcal{V}$ and $\mathcal{P}$ requires a lot of bandwidth

✗ $\mathcal{V}$ and $\mathcal{P}$ on circuit board? Too much energy, circuit area

Protocol requires input-independent precomputation [Allspice13]

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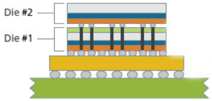

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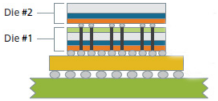

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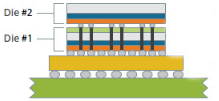

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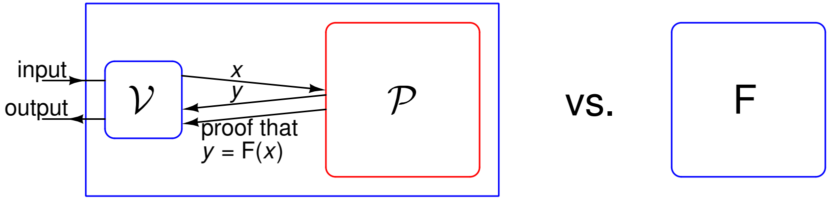
Several other details (see paper)

Implementation

Zebra's implementation includes

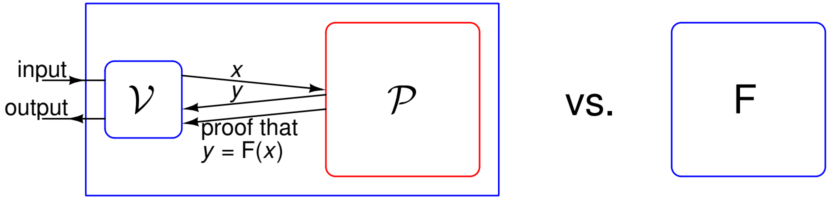
- a compiler that produces synthesizable Verilog for $\mathcal{P}$
- two $\mathcal{V}$ implementations
  - hardware (Verilog)
  - software (C++)
- library to generate $\mathcal{V}$'s precomputations
- Verilog simulator extensions to model software or hardware $\mathcal{V}$'s interactions with $\mathcal{P}$

Evaluation method



Baseline: direct implementation of F in same technology as $\mathcal{V}$

Evaluation method



Baseline: direct implementation of F in same technology as $\mathcal{V}$

Metrics: energy, chip size per throughput (see paper)

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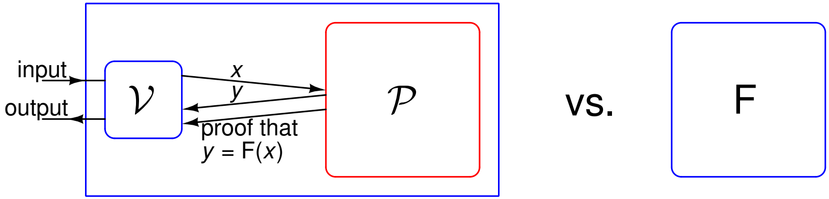

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Measurements: based on circuit synthesis and simulation, published chip designs, and CMOS scaling models

Charge for $\mathcal{V}$, $\mathcal{P}$, communication; retrieving and decrypting precomputations; PRNG; Operator communicating with $\mathcal{V}$

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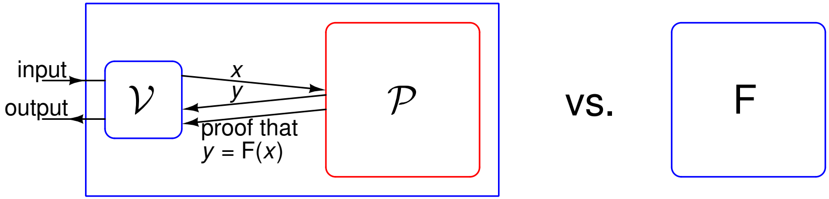

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350 nm: 1997 (Pentium II)
7 nm: $\approx$ 2017 [TSMC]
$\approx$ 20 year gap between
trusted and untrusted fab

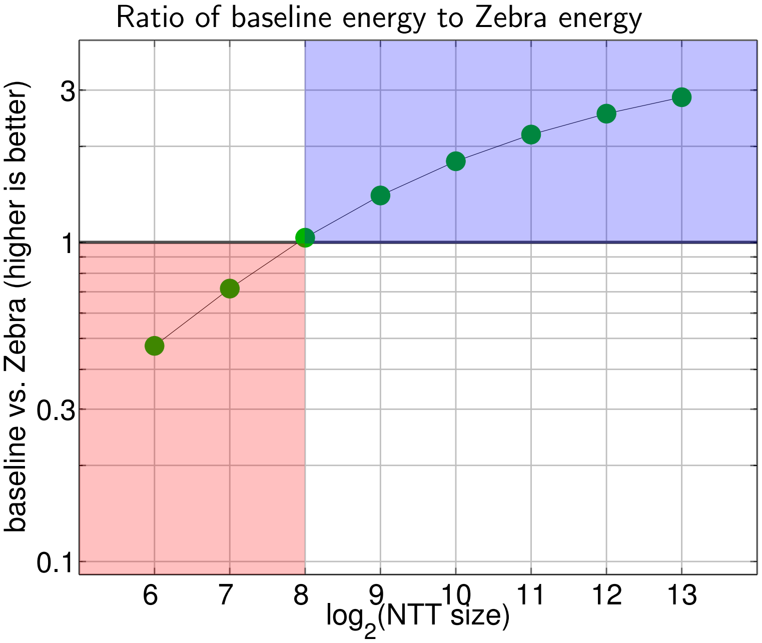
Constraints: trusted fab = 350 nm; untrusted fab = 7 nm
200 mm^2 max chip area; 150 W max total power

Application #1: number theoretic transform

NTT: a Fourier transform over $\mathbb{F}_p$

Widely used, e.g., in computer algebra

Application #1: number theoretic transform

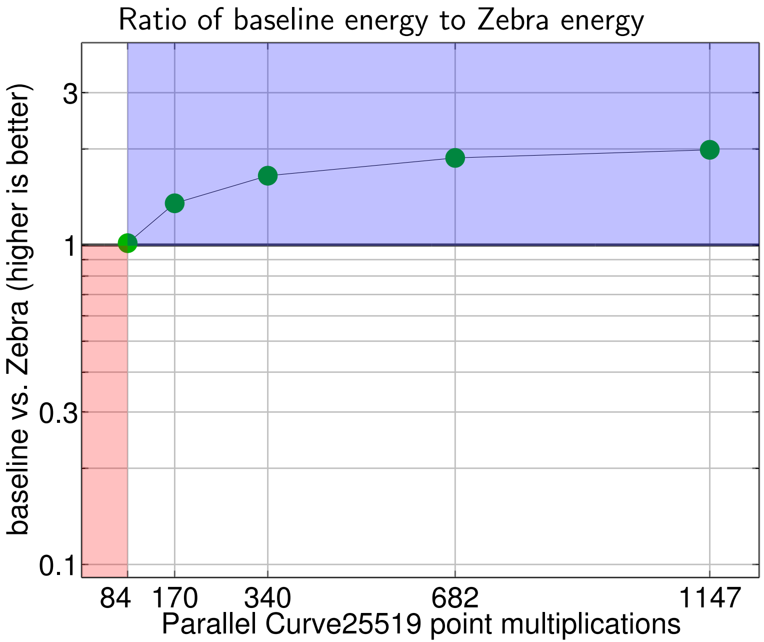


Application #2: Curve25519 point multiplication

Curve25519: a commonly-used elliptic curve

Point multiplication: primitive used for ECDH

Application #2: Curve25519 point multiplication



A **qualified** success

Zebra: a hardware design that saves costs...

...**sometimes**.

Summary of Zebra's applicability

1. Must have a wide gap between cutting-edge fab for $\mathcal{P}$ and trusted fab for $\mathcal{V}$
2. Must amortize precomputations over many instances
3. Computation F must be very large for $\mathcal{V}$ to save work
4. Computation F must be efficient as an arithmetic circuit
5. Computation F must have a layered, shallow, deterministic AC

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Applies to IPs, but not arguments

Arguments versus IPs, redux

Design principle	**IPs** [GKR08, CMT12, VSBW13]	**Arguments** [GGPR13, SBVBPW13, PGHR13, BCTV14]
Extract parallelism	✓	✓
Exploit locality	✓	
Reduce, reuse, recycle	✓	

Argument protocols seem friendly to hardware?

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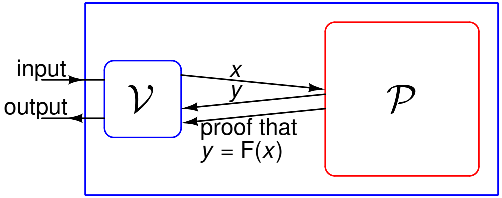
. . . but we hope these issues are surmountable!

Recap



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- First hardware design for a probabilistic proof protocol
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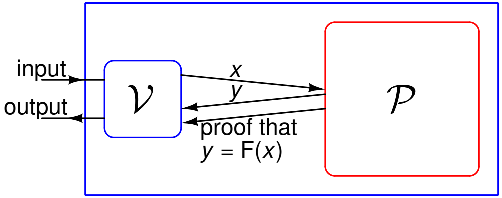

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  large gap between trusted and untrusted technology
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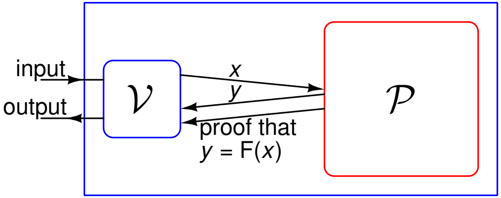

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https://www.pepper-project.org/